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1/1 DWPX - (C) Thomson Derwent

AN - 1985-053464 [09]

TI - Reduced carrier transient time semiconductor device - forms spike  
barrier in valance band on hetero-junction surface between emitter  
and base **NoAbstract Dwg 2/4**

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# PATENT ABSTRACTS OF JAPAN

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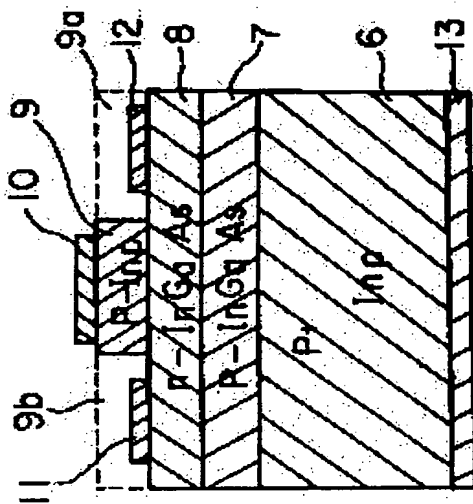
(21)Application number : 58-119080

(71)Applicant : FUJITSU LTD

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## (54) SEMICONDUCTOR DEVICE



### (57)Abstract:

**PURPOSE:** To inject holes of high speed to a base, and to shorten the transient time of a small number of carriers by forming spiky barriers to a valence band in an emitter-base junction section and passing the barriers through holes, mobility thereof is originally low.

**CONSTITUTION:** A first layer p type InGaAs layer 7 is formed on an InP p+ substrate 6, and an n type InGaAs layer 8 is formed on the p type -InGaAs layer and a p type InP layer 9 further on the layer 8. AuGe/Au electrodes 11, 12 as base electrodes are formed on the second layer n-InGaAs layer 8 through etchings 9a, 9b up to the second layer n type InGaAs layer while leaving an emitter region in the third layer InP layer. Ohmic contacts are formed through alloyings to form bases, Au/Zn/Au electrodes 10, 13 are shaped to the third layer p type InP layer 9 and the back of a p+ type InP 6, and emitter and collector electrodes are formed through the making of ohmics. Accordingly, a p-n-p hetero-junction bipolar transistor is formed.

## LEGAL STATUS

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